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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,776	09/30/2003	Jimmie Earl DeWitt JR.	AUS920030481US1	6262
35525	7590	03/06/2007	EXAMINER	
IBM CORP (YA)			VU, TUAN A	
C/O YEE & ASSOCIATES PC				
P.O. BOX 802333			ART UNIT	PAPER NUMBER
DALLAS, TX 75380			2193	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

## Office Action Summary

Application No.

10/675,776

Applicant(s)

DEWITT ET AL.

Examiner

Tuan A. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 9/30/03 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 9/30/03.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- ☐ Notice of Informal Patent Application
- ☒ Other: See Continuation Sheet.

Continuation of Attachment(s) 6). Other: IDS:

7/1/05;1/9/06;1/30/06;2/14/06;3/27/06;4/25/06;5/26/06;6/5/06;6/23/06;6/26/06;8/3/06;8/18/06;10/2/06;11/2/06;12/4/06;1/22/07

DETAILED ACTION

1. This action is responsive to the application filed 12/17/2003.

Claims 1-25 have been submitted for examination.

*Information Disclosure Statement*

2. The information disclosure statement filed 9/30/03; 7/1/05; 1/9/06; 1/30/06; 2/14/06; 3/27/06; 4/25/06; 5/26/06; 6/5/06; 6/23/06; 6/26/06; 8/3/06; 8/18/06; 10/2/06; 11/2/06; 12/4/06; 1/22/07 amounts to retrieving unfiltered data coming from many apparent PTO-892 forms provided by previous or ongoing Office Actions (effectuated by many examiners) working of related cases, and do not particularly address and have significant relevance the instant subject matter being disclosed -- for the most part; which otherwise signifies a huge burden on the Examiner's part in terms of reviewing all cited documents; hence as a whole, fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance; as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein, although marked as CONSIDERED, has actually been considered only with little weight (or with no merits at all) until Applicants provide statement as to (each and all of) their respective relevance to the instant claimed invention. About which, some of the IDS are identified with some deficiency, as follows.

3. The information disclosure statement filed 9/30/2003 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of some cited foreign patent document, namely items BP, item BQ at pg. 2, none provided with a copy; each non-patent literature publication or that

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portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file and partially considered, but the identified information referred to from above has not been considered, nor has item **BH** ( all non-considered will be marked with NC) which is a Japanese version without any form of translation.

4. Likewise, the IDS filed 2/14/2006 also fails to comply to the CFR 1.98 as item AC is not provided with a correct copy listed as 'Introduction Using the Intel 80C188EB'. It has been placed in the application file and partially considered, but the information referred to indicated above has not been considered ( marked with NC) as to the merits.

Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

#### ***Specification***

5. The Specifications objected to because of the following informalities: The Cross Reference section ( pg. 1) needs to be readjusted whenever possible to provide more proper or current U.S. Application Number in place of the blank spaces corresponding to the related Attorney docket number. Appropriate correction is suggested but any subsequent outcome will not be held in abeyance.

#### ***Double Patenting***

6. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed.

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Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1, 13, 21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 20, 25 of copending Application No. 10/675777 (hereinafter '777).

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per instant claims 1, 13, 21, '777 claims 3, 20, 25 also recite determining for a instruction during execution for a association of an indicator; associating a counter based on such determination and incrementing a counter in response to the indicator association with the instruction. The event counting as recited by '777 is construed as obvious representation to a runtime indicator (leading to a counter increment) of the instant claims.

8. Claims 1, 13, 21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 19, 23, 25 of copending Application No. 10/675778 (hereinafter '778). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per claims 1, 13, 21, '778 claims 1, 9, 19, 23, 25 recites an execution environment wherein upon determining that an indicator (Note: even though '778 does not recite indicator per

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se, a threshold exceeding point can be conceived as a runtime indicator) is associated with an instruction, counting execution of such instruction based on such indicator. Even though '778 recites that the indicator is a threshold value event, this limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented in view of the above association.

9. Claims 1, 13, 21 and 10, 18, 25 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 16 of copending Application No. 10/675872 (hereinafter '872).

As per instant claims 1, 13, 21, '872 claims 2, 16 also recite determining whether an instruction in execution is related with an runtime 'indicator' (Note: even though '872 does not recite indicator per se, a point in a memory range can be analogous to a runtime indicator); and counting each event associated with the instruction if the instruction is associated with that indicator. Even though '778 recites that the indicator is a point in contiguous range, this limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented in view of the above association.

As per instant claims 10, 18, 25, '872 claims 2, 16 also recite determining whether a memory access instruction is associated with a 'memory location' (Note: even though '872 does not recite memory location per se, a point in a memory range can be analogous to a location); and counting each event associated with the instruction if the instruction is associated with that determination. Even though '872 explicitly recites that the indicator is a location within contiguous range, this location-within- range limitation would be a obvious representation of any

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runtime indicator that would characterizes as an event deemed for the counter to be incremented in view of the above association determination.

10. Claims 1, 13, 21 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 17 of copending Application No. 10/675721 (hereinafter '721).

As per instant claims 1, 13, 21, '721 claims 1, 9, 17 also recite determining for a instruction during execution for a association of a indicator ( Note: even though '721 does not recite an indicator per se, a set of indicators can be analogous to one such runtime indicator) ; incrementing a counter in response to the indicator association with the instruction. The instruction in the *routine of interest* as recited by '721 is construed as obvious representation to a runtime instruction that requires some action (e.g. to monitor or to trace/modify leading to a counter increment) of the instant claims.

11. Claims 10, 18, 25 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 9, 17 of copending Application No. 10/682385 (hereinafter '385).

As per instant claims 10, 18, 25, '385 claims 1, 12, 23 also recite determining whether a memory access instruction is associated with a indicator (Note: even though '385 recites data values in memory specifying counting event, a runtime event such as those memory indicators can be analogous to on runtime indicator of the instant claim); and counting each event associated with the instruction if the instruction is associated with that memory location in view of the indicator. Even though '385 explicitly recites that counting events associated with execution based on detection of value indicators, this limitation would be a obvious



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representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented in view of the above association determination.

### ***Claim Objections***

12. Claims 4, 16, 24 are objected to because of the following informalities: the language recited as 'incrementing the counter by an instruction cache' does not appear interpretable with regard to accepted meaning of a instruction cache, nor is it commensurate with the teaching about the counter relationship with this cache in the Disclosure. The Specifications (e.g. Specifications - pg. 23-24) teach signals or instructions including indicators communicated between the cache, some decoder scheduler and a Performance monitoring unit, so that a counter inside the performance monitor unit can be incremented by way of analyzing specific structural parts of the instruction/indicator sent from the above cache. Appropriate correction is required lest this become a non-enablement or non-statutory type of rejection.

### ***Claim Rejections - 35 USC § 101***

13. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

14. Claims 1-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The Federal Circuit has recently applied the practical application test in determining whether the claimed subject matter is statutory under 35 U.S.C. § 101. The practical application test requires that a "useful, concrete, and tangible result" be accomplished. An "abstract idea" when practically applied is eligible for a patent. As a consequence, an invention, which is eligible for patenting under 35 U.S.C. § 101, is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The test for practical application is thus to determine whether the claimed invention produces a "useful, concrete and tangible result".

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Specifically, claims 1, 13, and 21 recite a method or system with means for determining if an instruction is associated with an indicator; and incrementing the counter if the instruction is executing and is associated with the indicator. The (method and system) step actions as claimed merely result in incrementing a counter thus do not amount to a concrete, tangible and useful result in the domain of application level of computer technologies, because a execution counter being internal and volatile with respect to a runtime, cannot be construed as a tangible and persisted result of any use. Moreover, the incrementing step is recited as being conditioned by of an indicator associated with the instruction, the potential absence of which (association) could lead to no incrementing being done at all; hence the claim as a whole leads to a no realization of any application-level useful and tangibly concrete result. Claims 1, 13, and 21 are rejected for leading to a non-statutory subject matter

Claims 10, 18, and 25 also recite method and system with means for determining association of a memory location with an indicator, and responsive to which increment a counter. These claim lacks reasonable conveying of a application result being realized, for the steps recited in these claims amount to merely accomplishing an internal volatile data, which is deemed non tangible in the level of real-world application; and the condition imposed by the possibility of an association is conveying that potentially no incrementing would be done. Therefore, as above, claims 10, 18, and 25 are rejected for leading to a non-statutory subject matter.

Claims 2-9, 11-12, 14-17, 19-20, 22-24 fail to cure to the deficiency of the base claims; hence are also rejected for leading to a non-statutory subject matter.

***Claim Rejections - 35 USC § 112***

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15. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

16. Claims 4, 16, 24 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: 'by an instruction cache' and 'incrementing the counter'. The implementation or structural specifics leading to construing 'incrementing the counter by an instruction cache' are not reasonably enabling the understanding as to how a cache can increment a counter, absent any signal or directive being invoked. From the disclosure (e.g. Specifications - pg. 23-24), it is construed that cache for storing instruction (Specifications - Fig. 2-4) is disclosed as sending to a performance monitor unit 306, and that marking of some instructions (Fig. 7) can be based upon by the performance monitor unit to increment a counter. The claim present a void or a gap that would otherwise enable one skilled in the art to see how a instruction storage can more or less cause a counter to be incremented. But 'incrementing a counter by an instruction cache' requires establishing a context requiring the following: what type or source of instruction is required, or directly executing, for causing the incrementing; where the counter is located; by what means the cache supports this counter incrementing; what signaling directive – path flow thereof from the cache to a counter – is acting upon a counter so that any incrementing instruction is performed. The claim language is unclear, devoid of crucial insight, and/or largely non-commensurate with the teaching of the Disclosure. Because of the above omission, the limitation will be treated as though by means of a interacting with a cache instruction, a counter

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can be incremented. Correction is required lest this leads to a lack of enabling description type of rejection.

***Claim Rejections - 35 USC § 102***

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Gover et al.,  
USPN: 5,752,062(hereinafter Gover)

**As per claim 1**, Gover discloses a method in a data processing system for monitoring execution of instructions, the method comprising: determining whether an instruction is associated with an indicator (e.g. Fig. 5; *count number, bit fields, MMCRO* - col. 10, lines 31-35; Fig. 6A; col. 11, line 62 to col. 12, line 42); and incrementing a counter associated with the instruction (e.g. *even... to be recorded/counted, counter ... selection, counter freeze* - col. 8, lines 41-50; col. 10, lines 53-63; col. 11 lines 14-50) in response to detecting execution of the instruction and to a determination that the instruction is associated with the indicator.

**As per claim 2**, Gover discloses resetting the counter if the counter exceeds a threshold value (e.g. *reset* - col. 12, lines 4-42).

**As per claim 3**, Gover discloses reading a value of the counter prior to the counter exceeding the threshold value (e.g. *enabled ... when low ... exception is signaled* – col. 11, lines 29-37 --Note: interrupt based upon exceeding of a number reads on reading a state and a counter value prior to such interrupt event – see col. 9 lines 16-20).

**As per claim 4**, Gover discloses incrementing the counter by an instruction cache (Fig. 2; col. 9, lines 10-56; Fig. 4-5 – Note: performance monitor unit for tracking number to trigger an interrupt in conjunction with state registers related to instruction to be rescheduled – see Fig. 1 -- reads on in response to indicator and instruction cache and execution of instruction related to indicator) in response to detecting execution of the instruction and to a determination that the instruction is associated with the indicator.

**As per claim 6**, Gover discloses wherein the counter is located in a shadow memory (e.g. col. 8, lines 26-39 – Note: special registers with state or content – MMCRn -- maintained via special privilege access mode and being kept in parallel with execution scheduling – see col. 11, lines 14-50 -- as informational support thereof, hence reads on shadowing type of information kept in memory; see SSR col. 9 lines 36-57).

**As per claims 5 and 7**, Gover discloses wherein the counter is a field (Fig. 6a-b) in the instruction; that the indicator is the counter ( Fig. 6a-b; col. 11-12).

**As per claim 8**, Gover discloses changing the indicator to disable counting (e.g. *user may determine* - col. 10 line 64 to col. 11, line 46; *user selectable* - col. 12, line 59 to col. 13, line 16) execution of the instruction upon subsequently encountering the indicator.

**As per claim 9**, Gover discloses wherein the determining step (e.g. Fig. 1, 4-5 and related text; col. 11-12; Fig. 6a-b) is initiated when the instruction is executed.

**As per claim 10**, Gover discloses a method in a data processing system for monitoring access to data, the method comprising:

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responsive to an access to a memory location (e.g. *data accesses* – col 10, lines 17-23), determining whether the memory location is associated with an indicator (e.g. Fig. 3-5; col. 8, lines 26-39; col. 11, lines 14-50); and

responsive to the memory location being associated with the indicator, incrementing a counter associated with the memory location (e.g. col. 8, lines 41-50; col. 11-12).

**As per claims 11-12**, Gover discloses wherein the counter is located in a field; wherein the field includes a control bit that forms the indicator (e.g. Fig. 6a-b).

**As per claim 13**, Gover discloses a data processing system for monitoring execution of instructions, the data processing system comprising: determining means for determining whether an instruction is associated with an indicator; and incrementing means for incrementing a counter associated with the instruction in response to detecting execution of the instruction and to a determination that the instruction is associated with the indicator;

all of which limitations having been addressed in claim 1.

**As per claims 14-17**, refer to the corresponding rejection as set forth in claims 2-4, 8 respectively.

**As per claim 18**, Gover discloses a data processing system in a data processing system for monitoring access to data, the data processing system comprising: determining means, responsive to an access to a memory location, for determining whether the memory location is associated with an indicator; and incrementing means, responsive to the memory location being associated with the indicator, for incrementing a counter associated with the memory location;

all of which limitations having been addressed in claim 10.

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**As per claims 19-20**, refer to the corresponding rejection as set forth in claims 11-12 respectively.

**As per claim 21**, Gover discloses a computer program product in a computer readable medium for monitoring execution of instructions, the computer program product comprising:

first instructions for determining whether an instruction is associated with an indicator;  
and

second instructions for incrementing a counter associated with the instruction in response to detecting execution of the instruction and to a determination that the instruction is associated with the indicator ( refer to corresponding rejection as set forth in claim 1)

**As per claims 22-24**, refer to the corresponding rejection as set forth in claims 2-4 respectively.

**As per claim 25**, Gover discloses computer program product in a computer readable medium for monitoring access to data, the computer program product comprising: first instructions for determining whether the memory location is associated with an indicator, responsive to an access to a memory location; and second instructions for incrementing a counter associated with the memory location, responsive to the memory location being associated with the indicator (refer to corresponding rejection as set forth in claim 10).

### ***Conclusion***

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 ( for non-official correspondence - please consult Examiner before using) or 571-273-8300 ( for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tuan A Vu  
Patent Examiner,  
Art Unit 2193  
March 01, 2007